Use QFN to get CSP

Chip Scale Packaging (CSP) is about bringing the package size as close as possible to the die size. The JEDEC defined QFN outline is a good alternative for low cost chip scale packages. Several different QFN-style package families are commercially available both for ASIC and for standard components.

The picture above shows an example of a QFN package. The Die is attached to a metal leadframe. Connections to the leads are made by wire bonding. The Die and the leadframe are covered by epoxy to form the assembled component. The leadframes come in sheets that will finally be a large number of components. Die attach, wire bond and epoxy moulding is performed “per sheet”. The components are then separated from each other by sawing.

**Quad Flat No lead**

The main advantage with a QFN compared to for example a Quad Flat Pack (QFP) when considering chip scale packaging is that the leads on the QFN are very short and do not extend outside the package body. A realistic distance from die edge to package footprint edge may be just less than 1 mm. The same distance for a QFP is at least around 3 mm. A QFN with its metal die-attach pad extending to the bottom side of the package also has excellent thermal properties.

QFN packages are defined in both rectangular and square versions and in sizes from 2 by 2 to 12 by 12 mm. The lead pitch is normally 0.5 mm. Lead-free and in other aspects RoHS compliant materials are available.

**Chip On Lead**

One further step towards CSP is to mount the Die directly onto the leads. This technique is called Chip On Lead (COL). The Die is supported by the leads and not by a separate die-attach pad. A die attach pad connected to at least one lead may be present. The die-attach material must then of course also be non-conducting. The die to package edge distance can now be in the range of 0.5 mm.

**Flip Chip On Lead**

Next milestone is to introduce flip-chip mounting instead of wire bonding. This technique is called Flip-Chip On Lead (FCOL). The lead frame must in most cases be custom made to fit the Die but this approach will give the smallest possible package. A die to package distance in the range of 0.2 mm is realistic.

QFN-style packages are used for all kind of applications. All the above QFN alternatives will give CSP or at least near-CSP performance as long as the number of connections is not very high. A component where the number of leads determines the package size may need a Ball Grid Array approach to get CSP performance.

The introduction of an ASIC will make it possible to select the best assembly alternative. There is always an assembly solution available if package density is an issue.